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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/644,133

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Chris P. Karamatas

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LAW OFFICES OF MICHAEL DRYJA

704 228TH AVE. NE

# 694

SAMMAMISH, WA 98074

EXAMINER

SPITTLE, MATTHEW D

ART UNIT

PAPER NUMBER

2111

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/644,133	<b>Applicant(s)</b> KARAMATAS ET AL.	
	<b>Examiner</b> Matthew D. Spittle	<b>Art Unit</b> 2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 02 August 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-10, 12-19 and 21-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10, 12-19 and 21-30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

Claims 1 – 30 have been examined.

#### ***Claim Rejections - 35 USC § 112***

5       The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10       Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite  
for failing to particularly point out and distinctly claim the subject matter which applicant  
regards as the invention.

Claim 10 recites the limitation "the interrupt-assignment software" in line 2.  
There is insufficient antecedent basis for this limitation in the claim.

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#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all  
obviousness rejections set forth in this Office action:

20       (a) A patent may not be obtained though the invention is not identically disclosed or described as set  
forth in section 102 of this title, if the differences between the subject matter sought to be patented and  
the prior art are such that the subject matter as a whole would have been obvious at the time the  
invention was made to a person having ordinary skill in the art to which said subject matter pertains.  
Patentability shall not be negated by the manner in which the invention was made.

25

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148  
USPQ 459 (1966), that are applied for establishing a background for determining  
obviousness under 35 U.S.C. 103(a) are summarized as follows:

Art Unit: 2111

- 30
1. Determining the scope and contents of the prior art.
  2. Ascertaining the differences between the prior art and the claims at issue.
  3. Resolving the level of ordinary skill in the pertinent art.
  4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

35           Claims 1 – 10, 12 – 19, and 21 – 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiick (U.S. Pub. 2003/0200250) in view of what is well known in the art as evidenced by Neal et al. (U.S. 6,347,349) and Carpenter et al. (U.S. 6,148,361).

          Regarding claim 1, Kiick teaches a method comprising at least one of:

40           Assigning interrupts for a plurality of input/output (I/O) devices among a plurality of nodes of a system based on at least one of: the nodes to which the I/O devices are connected; the nodes at which interrupt service routines for the I/O devices reside; and processors of the nodes for the nodes having processors, where one or more of the nodes have processors and memory (Paragraph 34 describes that interrupts should be

45   assigned to the “closest” processors, and not across node boundaries. Examiner interprets this to mean the interrupts for the I/O devices should be assigned to nodes to which they are connected or to nodes where the ISRs for the said I/O devices reside.);

          For each node of the system having processors, assigning the interrupts for the devices that are performance critical and that have been assigned to the node among

50   the processors of the node in a round-robin manner (Examiner interprets all devices in the reference to be considered “performance critical”; Paragraph 26);

Dynamically modifying assignments of the interrupts among the nodes of the system based on actual performance characteristics of the assignments (Paragraphs 25, 28, 31);

55        For each node of the system having processors, dynamically modifying assignments of the interrupts that are performance critical and that have been assigned to the node among the processors of the node based on actual performance characteristics of the assignments (Paragraphs 25, 28, 31).

60        Kiick fails to teach where one or more of the nodes are processorless and memoryless.

Examiner takes official notice that it is well known in this art to have nodes in NUMA systems that are memoryless and processorless, as evidenced by Neal et al. (Figure 1, item 122; column 1, lines 60 – 66; column 3, lines 1 – 3) and Carpenter et al. (Figure 1, item 8; column 12, lines 16 – 34).

65        With regard to claim 2, Kiick teaches the method of claim 1, wherein assigning the interrupts for the plurality of I/O device among the plurality of nodes of the system comprises, for each I/O device:

70        Where the node (Figure 1, items 102A, 102B) to which the I/O device (Figure 1, items 110A, 110B) is connected has a cache (Paragraph 10), memory (Figure 1, items 108A, 108B), and at least one processor (Figure 1, items 106A, 106B), assigning the interrupt for the I/O device to the node to which the I/O device is connected;

Otherwise, where the node at which the interrupt service routine for the I/O device resides has memory and at least one processor, assigning the interrupt for the I/O device to the node at which the interrupt service routine for the I/O device resides (Paragraph 34 describes that interrupts should be assigned to the “closest” processors, and not across node boundaries. Examiner interprets this to mean the interrupts for the I/O devices should be assigned to nodes to which they are connected or to nodes where the ISRs for the said I/O devices reside.).

With regard to claim 3, Kiick describes the method of claim 2, wherein assigning the interrupts for the plurality of I/O devices among the plurality of nodes of the system further comprises, for each I/O device, otherwise, assigning the interrupt for the I/O device to one of the nodes having memory and at least one processor (Paragraph 23 describes each node containing memory (Figure 1, items 108A, 108B), and at least one processor (Figure 1, items 106A, 106B); paragraph 26).

With regard to claim 4, Kiick teaches the method of claim 1, wherein dynamically modifying the assignments of the interrupts among the nodes of the system comprises:

Measuring responsiveness of the node in processing the interrupt (paragraphs 27 – 30);

Kiick fails to explicitly teach assigning the interrupt to the node at which the interrupt service routine for the I/O device resides; measuring responsiveness of the node at which the interrupt service routine for the I/O device resides in processing the

95 interrupt; and where the responsiveness of the node to which the I/O device is  
connected is better than the responsiveness of the node at which the interrupt service  
routine for the I/O device resides, reassigning the interrupt to the node to which the I/O  
device is connected.

Kiick does, however, teach that the dynamic interrupt distributor should be aware  
100 of the system architecture, and re-assign interrupts to the "closest" processors  
(paragraph 34). Therefore, it would have been obvious to one of ordinary skill in this art  
at the time of invention by Applicant to give preference in assigning interrupts to nodes  
at which the ISR for the device resides, or at which the I/O device itself resides, and  
then to re-assign interrupts accordingly to which configuration produced better  
105 performance as described in paragraphs 28 – 30).

With regard to claim 5, Kiick teaches the method of claim 4, wherein dynamically  
modifying the assignments of the interrupts among the nodes of the system comprises,  
for each assignment of an interrupt for an I/O device to a node, where the node is that  
110 at which the interrupt service routine for the I/O device resides:

Measuring responsiveness of the node in processing the interrupt (paragraphs  
27 – 30);

Kiick fails to explicitly teach assigning the interrupt to the node to which the I/O  
device is connected; measuring responsiveness of the node to which the I/O device is  
115 connected in processing the interrupt; and where the responsiveness of the node at  
which the interrupt service routine for the I/O device is connected is better than the

responsiveness of the node to which the I/O device is connected, reassigning the interrupt to the node at which the interrupt service routine for the I/O device resides.

Kiick does, however, teach that the dynamic interrupt distributor should be aware  
120 of the system architecture, and re-assign interrupts to the “closest” processors  
(paragraph 34). Therefore, it would have been obvious to one of ordinary skill in this art  
at the time of invention by Applicant to give preference in assigning interrupts to nodes  
at which the I/O device is connected, or at which the ISR for the I/O device itself resides,  
and then to re-assign interrupts accordingly to which configuration produced better  
125 performance as described in paragraphs 28 – 30).

With regard to claim 6, Kiick teaches the method of claim 1, wherein for each  
node of the system, dynamically modifying the assignments of the interrupts that are  
performance critical and that have been assigned to the node among the process ors of  
130 the node comprises:

Measuring the responsiveness of the processors of the node in processing the  
interrupts assigned thereto (paragraphs 27, 28, 35);

Where a differential between a best responsiveness and a worst responsiveness  
is greater than a threshold (paragraph 28; where a threshold may be interpreted as a  
135 “large enough difference”);

Reassigning at least one of the interrupts assigned to the processor having the  
worst responsiveness to the processor having the best responsiveness (paragraphs 27  
– 30, 35).



140           With regard to claim 7, Kiick teaches a non-uniform memory access (NUMA)  
system comprising:

          A plurality of nodes (Figure 1, items 102A, 102B);

          A plurality of input/output (I/O) devices, each I/O device connected to one of the  
plurality of nodes and having an interrupt (Figure 1, items 110A, 110B);

145           An interrupt-assignor responsive to the I/O devices and the nodes to assign the  
interrupt for each I/O device to one of the plurality of nodes in a performance-optimized  
manner (where an interrupt-assignor may be interpreted as a dynamic interrupt  
distributor; Figure 2, item 210; paragraphs 25, 28).

          Kiick teaches a multiprocessor system that is tightly-coupled, and could have  
150   shared main memory, mass storage, and cache, and runs a single copy of an operating  
system (paragraph 7). These limitations define a NUMA system as evidenced by the  
definition fromt5 Whatis.com, and therefore, Kiick implicitly describes a NUMA system  
for use with his invention.

          Kiick fails to teach where one or more of the nodes are processorless and  
155   memoryless.

          Examiner takes official notice that it is well known in this art to have nodes in  
NUMA systems that are memoryless and processorless, as evidenced by Neal et al.  
(Figure 1, item 122; column 1, lines 60 – 66; column 3, lines 1 – 3) and Carpenter et al.  
(Figure 1, item 8; column 12, lines 16 – 34).

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With regard to claim 8, Kiick teaches the system of claim 7, wherein the memory of each node that has memory is local to the node and remote to all other nodes (Figure 1, items 108A, 108B; paragraph 23 describes each domain having domain-specific memory (where a domain may be interpreted as a node, as described earlier in paragraph 23)), and the interrupt-assignor is to assign the interrupt for each I/O device to one of the plurality of nodes that has memory and at least one processor (where an interrupt-assignor may be interpreted as a dynamic interrupt distributor; Figure 2, item 210; paragraphs 25, 28; all nodes (items 102A, 102B are shown in Figure 1 to have memory and at least one processor).

With regard to claim 9, Kiick teaches the system of claim 8, wherein at least one of the I/O devices are performance critical, the interrupt-assignor further to assign the interrupt for each I/O device that is performance critical among the at least one processor of the node to which the interrupt has been assigned in a round-robin manner (Examiner interprets all of the I/O devices of the invention of Kiick to be performance critical, thereby necessitating the use of his invention to improve performance; Paragraphs 25, 26, 28).

With regard to claim 10, Kiick describes the system of claim 7, wherein, for each node that has processors, the interrupt-assignment software is further to dynamically modify assignments of the interrupts that are performance critical among the at least one processor of the node based on actual performance characteristics of the

assignments. Examiner believes Applicant meant to refer to "the interrupt-assignor" instead of "interrupt-assignment software." (Paragraphs 26, 28, 31).

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With regard to claim 12, Kiick describes the system of claim 7, wherein the interrupt-assignor is further to dynamically modify assignments of the interrupts among the plurality of nodes based on actual performance characteristics of the assignments (Paragraphs 26, 28, 31).

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Regarding claim 13, Kiick teaches wherein the interrupt-assignor (paragraph 34, where a interrupt-assignor may be interpreted as a dynamic interrupt distributor) is to give primary preference in assigning the interrupt for each I/O device to the node to which the I/O device is connected (paragraph 34, where a domain may be interpreted as a node) where the node to which the I/O device is connected has a cache (paragraph 10; Examiner interprets the processors within the processor complex (106A, 106B) as having on-chip cache), memory (Figure 1, items 108A, 108B) , and at least one processor (Figure 1, items 106A, 106B).

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Regarding claim 14, Kiick teaches wherein each I/O device further has an interrupt service routine residing at one of the plurality of nodes, and the interrupt-assignor (paragraph 34, where a interrupt-assignor may be interpreted as a dynamic interrupt distributor) is to give secondary preference in assigning the interrupt for each I/O device to the node at which the interrupt service routine of the I/O device resides

205 (paragraphs 28, 34; Examiner notes that paragraph 28 identifies re-assigning interrupts  
to be equivalent to re-assigning ISRs) where the node at which the interrupt service  
routine of the I/O device resides has a cache (paragraph 10; Examiner interprets the  
processors within the processor complex (106A, 106B) as having on-chip cache),  
memory (Figure 1, items 108A, 108B), and at least one processor ((Figure 1, items  
210 106A, 106B).

With regard to claim 15, Kiick describes the system of claim 7, wherein the  
interrupt-assignor resides within one of the plurality of nodes (where an interrupt-  
assignor may be interpreted as a dynamic interrupt distributor; Figure 2, item 210;  
215 paragraph 28 describes a predetermined processor in a domain (node) dedicated to run  
the interrupt-assignor).

With regard to claim 16, Kiick teaches an article of manufacture comprising:

A computer readable medium;

220 Means in the medium for assigning interrupts for a plurality of input/output (I/O)  
devices (paragraph 28 describes a dynamic interrupt distributor embodied as a program  
module. Examiner identifies that a program module must be embodied on a computer  
readable medium in order to be useful, and therefore implicitly describes this limitation)  
among a plurality of nodes based on at least one factor selected from the set consisting  
225 of: the nodes to which the devices are connected, and the nodes at which interrupt  
service routines for the I/O devices reside (Paragraph 34 describes that interrupts

should be assigned to the "closest" processors, and not across node boundaries.

Examiner interprets this to mean the interrupts for the I/O devices should be assigned to nodes to which they are connected or to nodes where the ISRs for the said I/O devices  
230 reside.), where one or more of the nodes have processors and memory.

Kiick fails to teach where one or more of the nodes are processorless and memoryless.

Examiner takes official notice that it is well known in this art to have nodes in NUMA systems that are memoryless and processorless, as evidenced by Neal et al.

235 (Figure 1, item 122; column 1, lines 60 – 66; column 3, lines 1 – 3) and Carpenter et al. (Figure 1, item 8; column 12, lines 16 – 34).

With regard to claim 17, Kiick teaches the article of claim 16, wherein the means is for assigning the interrupts among the plurality of nodes further based on whether the  
240 nodes have processors and memories (Kiick describes assigning ISRs to processors which have associated memories; paragraph 14).

With regard to claim 18, Kiick describes the article of claim 16, wherein the means, for each node having processors, is further for assigning the interrupts for the  
245 devices that are performance critical and that have been assigned to the node among the processors of the node in a round-robin manner (Examiner interprets all of the I/O devices of the invention of Kiick to be performance critical, thereby necessitating the use of his invention to improve performance; Paragraphs 25, 26, 28).

250           With regard to claim 19, Kiick describes the article of claim 18, wherein the  
means, is further for dynamically modifying assignments of the interrupts among the  
nodes based on actual performance characteristics of the assignments, and, for each  
node having processors, for dynamically modifying assignments of the interrupts that  
are performance critical and that have been assigned to the node among the  
255   processors of the node based on actual performance characteristics of the assignments  
(paragraphs 25, 28, 31).

With regard to claim 21, teaches describes an article of manufacture comprising:

260           An interrupt-assignor (Figure 2, item 210; paragraph 28) to assign interrupts for a  
plurality of input/output (I/O) devices among a plurality of nodes based on at least one  
factor selected from the set consisting of:

The nodes to which the I/O devices are connected;

The nodes at which interrupt service routines for the I/O devices reside, where  
one or more of the nodes have processors and memory.

265           (Paragraph 34 describes that interrupts should be assigned to the “closest”  
processors, and not across node boundaries. Examiner interprets this to mean the  
interrupts for the I/O devices should be assigned to nodes to which they are connected  
or to nodes where the ISRs for the said I/O devices reside.).

270           Kiick fails to teach where one or more of the nodes are processorless and  
memoryless.

Examiner takes official notice that it is well known in this art to have nodes in NUMA systems that are memoryless and processorless, as evidenced by Neal et al. (Figure 1, item 122; column 1, lines 60 – 66; column 3, lines 1 – 3) and Carpenter et al. (Figure 1, item 8; column 12, lines 16 – 34).

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With regard to claim 22, Kiick teaches the article of claim 216, wherein the means is for assigning the interrupts among the plurality of nodes further based on whether the nodes have processors and memories (Kiick describes assigning ISRs to processors which have associated memories; paragraph 14).

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With regard to claim 23, Kiick teaches the article of claim 21, wherein the interrupt-assignor is to assign, for each node, the interrupts for the devices that are performance critical and that have been assigned to the node among the processors of the node in a round-robin manner (where the interrupt-assignor may be interpreted as a dynamic interrupt distributor; Examiner interprets all of the I/O devices of the invention of Kiick to be performance critical, thereby necessitating the use of his invention to improve performance; Paragraphs 25, 26, 28).

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With regard to claim 24, Kiick teaches the article of claim 23, wherein the interrupt-assignor is to dynamically modify assignments of the interrupts among the nodes based on actual performance characteristics of the assignments, and, for each node having processors, to dynamically modify assignments of the interrupts that are

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performance critical and that have been assigned to the node among the processors of the node based on actual performance characteristics of the assignments (where an interrupt-assignor may be interpreted as a dynamic interrupt distributor; paragraphs 25, 28, 31).

With regard to claim 25, Kiick teaches a method comprising:

Assigning interrupts for a plurality of input/output (I/O) devices among a plurality of nodes based on at least one factor selected from the set consisting of: the nodes to which the I/O devices are connected; and the nodes at which interrupt service routines for the I/O devices reside, where one or more of the nodes have processors and memory (Paragraph 34 describes that interrupts should be assigned to the "closest" processors, and not across node boundaries. Examiner interprets this to mean the interrupts for the I/O devices should be assigned to nodes to which they are connected or to nodes where the ISRs for the said I/O devices reside.);

For each node of the system, assigning the interrupts for the devices that are performance critical and that have been assigned to the node among the processors of the node in a round-robin manner (Examiner interprets all of the I/O devices of the invention of Kiick to be performance critical, thereby necessitating the use of his invention to improve performance; Paragraphs 25, 26, 28);

Dynamically modifying assignments of the interrupts among the nodes of the system based on actual performance characteristics of the assignments (paragraphs 25, 28, 31);



315 For each node of the system, dynamically modifying assignments of the  
interrupts that are performance critical and that have been assigned to the node among  
the processors of the node based on actual performance characteristics of the  
assignments (paragraphs 25, 28, 31).

Kiick fails to teach where one or more of the nodes are processorless and  
320 memoryless.

Examiner takes official notice that it is well known in this art to have nodes in  
NUMA systems that are memoryless and processorless, as evidenced by Neal et al.  
(Figure 1, item 122; column 1, lines 60 – 66; column 3, lines 1 – 3) and Carpenter et al.  
(Figure 1, item 8; column 12, lines 16 – 34).

325 With regard to claim 26, Kiick teaches the method of claim 25, wherein assigning  
the interrupts for the plurality of I/O devices among the plurality of nodes of the system  
comprises, for each I/O device:

Where the node (Figure 1, items 102A, 102B) to which the I/O device (Figure 1,  
330 items 110A, 110B) is connected has a cache (Paragraph 10), memory (Figure 1, items  
108A, 108B), and at least one processor (Figure 1, items 106A, 106B), assigning the  
interrupt for the I/O device to the node to which the I/O device is connected;

Otherwise, where the node at which the interrupt service routine for the I/O  
device resides has memory and at least one processor, assigning the interrupt for the  
335 I/O device to the node at which the interrupt service routine for the I/O device resides  
(Paragraph 34 describes that interrupts should be assigned to the "closest" processors,

and not across node boundaries. Examiner interprets this to mean the interrupts for the I/O devices should be assigned to nodes to which they are connected or to nodes where the ISRs for the said I/O devices reside.).

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With regard to claim 27, Kiick teaches the method of claim 25, wherein assigning the interrupts for the plurality of I/O devices among the plurality of nodes of the NUMA system further comprises, for each I/O device, otherwise, assigning the interrupt for the I/O device to one of the nodes having memory and at least one processor (Paragraph 23 describes each node containing memory (Figure 1, items 108A, 108B), and at least one processor (Figure 1, items 106A, 106B); paragraph 26).

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With regard to claim 28, Kiick teaches the method of claim 25, wherein dynamically modifying the assignments of the interrupts among the nodes of the system

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comprises:

Measuring responsiveness of the node in processing the interrupt (paragraphs 27 – 30);

Kiick fails to explicitly teach assigning the interrupt to the node at which the interrupt service routine for the I/O device resides; measuring responsiveness of the node at which the interrupt service routine for the I/O device resides in processing the interrupt; and where the responsiveness of the node to which the I/O device is connected is better than the responsiveness of the node at which the interrupt service

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routine for the I/O device resides, reassigning the interrupt to the node to which the I/O device is connected.

360           Kiick does, however, teach that the dynamic interrupt distributor should be aware of the system architecture, and re-assign interrupts to the "closest" processors (paragraph 34). Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to give preference in assigning interrupts to nodes at which the ISR for the device resides, or at which the I/O device itself resides, and  
365 then to re-assign interrupts accordingly to which configuration produced better performance as described in paragraphs 28 – 30).

With regard to claim 29, Kiick teaches the method of claim 25, wherein dynamically modifying the assignments of the interrupts among the nodes of the system  
370 comprises, for each assignment of an interrupt for an I/O device to a node, where the node is that at which the interrupt service routine for the I/O device resides:

Measuring responsiveness of the node in processing the interrupt (paragraphs 27 – 30);

Kiick fails to explicitly teach assigning the interrupt to the node to which the I/O  
375 device is connected; measuring responsiveness of the node to which the I/O device is connected in processing the interrupt; and where the responsiveness of the node at which the interrupt service routine for the I/O device is connected is better than the responsiveness of the node to which the I/O device is connected, reassigning the interrupt to the node at which the interrupt service routine for the I/O device resides.

380           Kiick does, however, teach that the dynamic interrupt distributor should be aware  
of the system architecture, and re-assign interrupts to the “closest” processors  
(paragraph 34). Therefore, it would have been obvious to one of ordinary skill in this art  
at the time of invention by Applicant to give preference in assigning interrupts to nodes  
at which the I/O device is connected, or at which the ISR for the I/O device itself resides,  
385   and then to re-assign interrupts accordingly to which configuration produced better  
performance as described in paragraphs 28 – 30).

          With regard to claim 30, Kiick teaches the method of claim 25, wherein for each  
node of the system having memory, dynamically modifying the assignments of the  
390   interrupts that are performance critical and that have been assigned to the node among  
the processors of the node comprises:

          Measuring the responsiveness of the processors of the node in processing the  
interrupts assigned thereto (paragraphs 27, 28, 35);

          Where a differential between a best responsiveness and a worst responsiveness  
395   is greater than a threshold (paragraph 28; where a threshold may be interpreted as a  
“large enough difference”);

          Reassigning at least one of the interrupts assigned to the processor having the  
worst responsiveness to the processor having the best responsiveness (paragraphs 27  
– 30, 35).

400

### ***Conclusion***

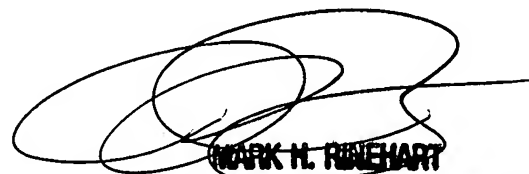
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

405 If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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**MARK H. RINEHART**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2100**